

Class.	Subclass	ISSUE CLASSIFICATION

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5397432

UTILITY SERIAL NUMBER	07/743,383	PATENT DATE	3/14/95	PATENT NUMBER	5,397,432
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SERIAL NUMBER	07/743,383	FILING DATE	08/21/91	CLASS	156	SUBCLASS		GROUP ART UNIT	1169	EXAMINER	
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**\*\*CONTINUING DATA\*\*\*\*\***  
VERIFIED

**\*\*FOREIGN APPLICATIONS\*\*\*\*\***  
VERIFIED PCT PCT/JP91/00861 06/26/91  
JAPAN 2-171791 06/27/90

Foreign priority claimed	<input type="checkbox"/> yes <input type="checkbox"/> no	AS FILED	STATE OR COUNTRY	SHEETS DRWGS.	TOTAL CLAIMS	INDER. CLAIMS	FILING FEE RECEIVED	ATTORNEY'S DOCKET NO.
35 USC 119 conditions met	<input type="checkbox"/> yes <input type="checkbox"/> no	→	JPX	6	22	4	\$560.00	911333
Verified and Acknowledged	Examiner's initials							

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**TITLE** METHOD FOR PRODUCING SEMICONDUCTOR INTEGRATED CIRCUITS AND APPARATUS  
USED IN SUCH METHOD

**CERTIFICATE**

U.S. DEPT. OF COMM./PAT. & TM—PTO-436L (Rev. 12)

JAN 19 1999

<b>PARTS OF APPLICATION FILED SEPARATELY</b>		<b>OF CORRECTION</b>		Applications Examiner	
<b>NOTICE OF ALLOWANCE MAILED</b>				<b>CLAIMS ALLOWED</b>	
		Assistant Examiner		Total Claims	Print Claim
<b>ISSUE FEE</b>				<b>DRAWING</b>	
Amount Due	Date Paid			Sheets Drwg.	Figs. Drwg.
				Print Fig.	
Label Area		Primary Examiner		<b>ISSUE BATCH NUMBER</b>	
		<b>PREPARED FOR ISSUE</b>			
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